ANALOG DEVICES

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APPLICATION NOTE

ONE TECHNOLOGY WAY • P.O. BOX 9106 • NORWOOD, MASSACHUSETTS 02062-9106 • 617/329-4700

Low-Cost, Two-Chip Voltage-Controlled Amplifier and Video Switch

by Charles Kitchin, Andrew Wheeler, and Ken Weigel

INTRODUCTION

Historically, it has been very difficult to build wide bandwidth, high quality, voltage-controlled amplifiers. Discrete designs have required a great deal of design effort while monolithic or hybrid integrated circuit approaches to VCA's have been expensive, or they have suffered from poor performance.

With the introduction of the AD539JN, a 60MHz analog multiplier in a plastic package, wideband gain-control is now practical at low cost. Used in conjunction with the 5539N wideband op-amp available from either Analog Devices or Signetics Corp. (also in a plastic package), the two devices can be connected together to create a high-speed voltage-controlled amplifier (VCA) or Video Switch with outstanding performance. In addition to providing a 50MHz bandwidth, this combination also satisfies even the most stringent differential phase and differential gain requirements. The AD539/5539 VCA is able to drive a 75Ω terminated coaxial cable directly.

A REVIEW OF SOME BASICS

Before describing the complete circuit, some basic principles of analog multiplication, as well as the main features of the AD539, will be reviewed. Monolithic multipliers have been commercially available since 1970, following the discovery of an important circuit design technique based on the logarithmic relationship between the base-emitter voltage of a bipolar transistor and its collector current. All IC multipliers now use this concept, known as the translinear principle.

One-quadrant multipliers accept input voltages at V_X and V_Y of only one polarity; accordingly, their operation is confined to quadrant 1 of a 4 quadrant X, Y coordinate system. This type of multiplier is of most use in high-accuracy computational roles.

Two-quadrant multipliers can accept voltages of either polarity at one of their input ports, but they can accept only a single polarity voltage at the other input. In gain-control applications, the bipolar input is considered the "signal" input and the single polarity input is referred to as the "control" input; therefore, when V_X is restricted to positive values, multiplier operation is confined to Quadrants 1 and 4.

Four-quadrant multipliers allow operation in all four quadrants with any combination of input polarity. Since this variety always preserves the correct sign at the output, it may at first seem that the four-quadrant type would *always* be the most useful variety of multiplier. However, this is *not* the case.

Until recently, the main emphasis in improving multiplier performance was directed toward higher precision, and four-quadrant operation was standard. However, the introduction of the AD539 two-quadrant multiplier deviates from this trend, by providing a 50MHz low distortion device optimized for gain control applications.

SOME ADVANTAGES OF TWO-QUADRANT MULTIPLIERS OVER OTHER TYPES

Four-quadrant analog multipliers have often been used in fast computational applications, in correcting the distortion of wide-angle CRT deflection systems, and in performing modulation and demodulation operations. However, in gain-control applications a two-quadrant multiplier is the better choice because this device is optimized for AC signals. This type of multiplier is often used for precision AGC, for implementing voltage-controlled amplifiers, and for creating various types of programmable filters.

Two-quadrant multipliers such as the AD539 have important advantages in gain-control applications, where there is no need (and it is undesirable) to respond to a bipolar control input voltage. Therefore, one functional advantage of the two quadrant multiplier is that the control channel can be fully blocked for all values of V_X below zero. As a practical matter, the offset voltage of the control channel can be made to be about one-tenth that of a general-purpose four-quadrant multiplier; this also provides improved low level gain accuracy.

Other advantages relate to improvements made possible in the design of the IC when the four-quadrant requirement is removed. In the AD539, these result in higher

bandwidth (60MHz versus 1MHz for a general-purpose device) with much smaller signal feedthrough at low gains, better phase response, lower signal-path distortion (the AD539 will generate less than 0.05% THD at full output in most applications), higher control-channel linearity, and lower noise (particularly at low gains).

TWO-SIGNAL CHANNELS WITH COMMON CONTROL

A unique feature of the AD539 is its own separate signal input channels, V_{Y1} and V_{Y2}, each with a nominal full-scale voltage range of $\pm 2V$ and each simultaneously controlled by a common input, V_X. V_X has a range of zero to $+3V$ FS. All inputs are referred to a common (input) ground connection.

The two-signal channels may be used in many different ways. First, of course, they can be used to control the magnitude of a pair of separate input signals. The excellent gain-tracking and high separation between channels of the AD539 proves to be valuable in this application; in fact, the bandwidth, crosstalk and other limitations occurring at high frequencies are caused more by the PC board layout than by the IC itself.

In applications where only a single channel is involved, the signal inputs and outputs may be connected in parallel. When driving grounded resistive loads, this configuration has the advantage of increasing the load power by a factor of four. Alternatively, the two-signal channels may be driven from complementary (phase and antiphase) signals, to achieve distortion figures as low as 0.01%; this mode is generally of more utility in low-speed applications (those with less than 1MHz bandwidth).

The two-signal channels may also be connected in series, thus providing a $V_X^2 V_Y$ function. This results in a circuit which has higher gain with twice the gain-control range (up to 100dB is practical) or instead, to provide a circuit with a more constant bandwidth over a reduced control voltage range. With the constant bandwidth circuit, the gain now varies as the square of the control voltage, which in some applications is advantageous.

A 50MHz VOLTAGE-CONTROLLED AMPLIFIER

Figure 1 is a circuit for a 50MHz voltage-controlled amplifier (VCA) suitable for use in high-quality-video-speed applications. The outputs from the two-signal channels of the AD539 (see "Inside the AD539" for a more complete circuit analysis) are applied to the op-amp in a subtracting configuration. This connection has two main advantages: first, it results in better rejection of the control voltage, particularly when over-driven ($V_X<0$ or $V_X>3.3V$). Secondly, it provides a choice of either non-inverting or inverting responses, using either inputs V_{Y1} or V_{Y2} respectively. In this circuit, the output of the op-amp will equal:

$$V_{OUT} = \frac{V_X (V_{Y1} - V_{Y2})}{2V} \text{ for } V_X > 0$$

Hence, the gain is unity at $V_X = +2V$. Since V_X can overrange to $+3.3V$, the maximum gain in this configuration is about 4.3dB. (Note: If pin 9 of the AD539 is grounded, rather than connected to the output of the 5539N, the maximum gain becomes 10dB.)

The bandwidth of this circuit is over 50MHz at full gain, and is not substantially affected at lower gains. Of course, when V_X is zero (or slightly negative, to override the residual input offset) there is still a small amount of capacitive feedthrough at high frequencies; therefore, *extreme* care is needed in laying out the PC board to minimize this effect. Also, for small values of V_X, the combination of this feedthrough with the multiplier output can cause a dip in the response where they are out of phase. Figure 2 shows the AC response from the non-inverting input, with the response from the inverting input, V_{Y2}, essentially identical. Test conditions: $V_{Y1} = 0.5V$ RMS for values of V_X from $+10mV$ to $+3.16V$; this is with a 75Ω load on the output. The feedthrough at $V_X = -10mV$ is also shown.

The transient response of the signal channel at $V_X = +2V$, $V_Y = V_{OUT} = +$ or $-1V$ is shown in Figure 3; with the VCA driving a 75Ω load. The rise and fall-times are both approximately 7ns.

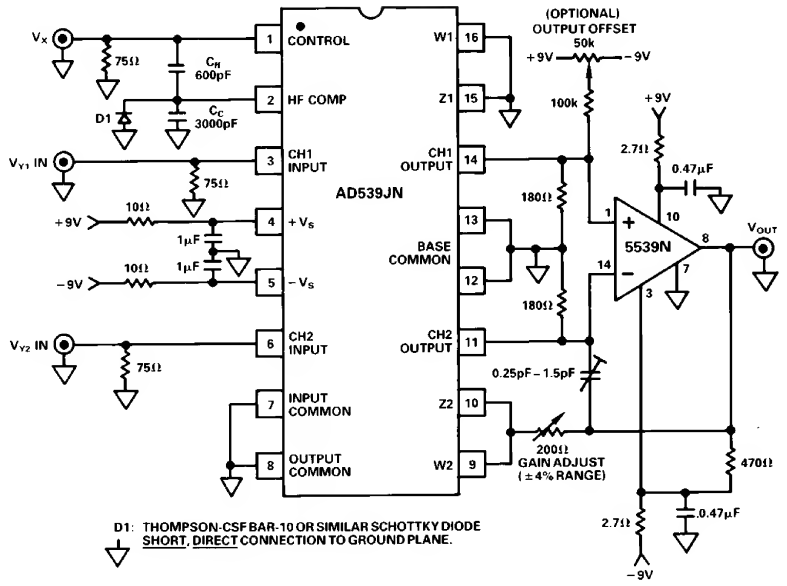

Figure 1. A Wide Bandwidth Voltage-Controlled Amplifier

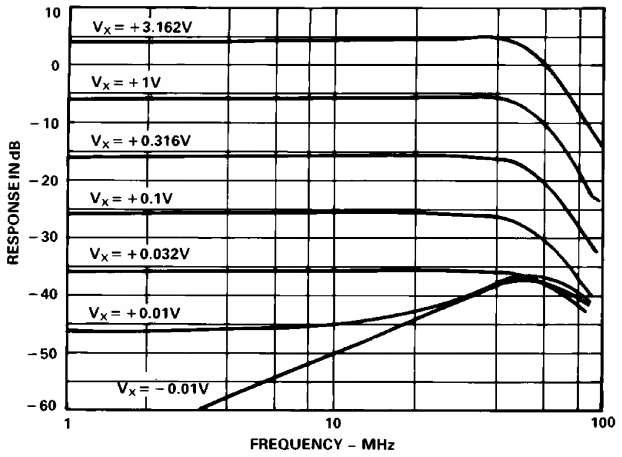

Figure 2. AC Response of the VCA at Different Gains $V_Y = 0.5V$ RMS

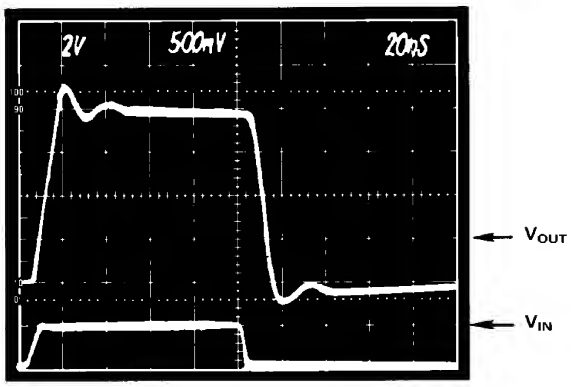

Figure 3. Transient Response of the Voltage-Controlled Amplifier $V_X = +2$ Volts, $V_Y = \pm 1$ Volt

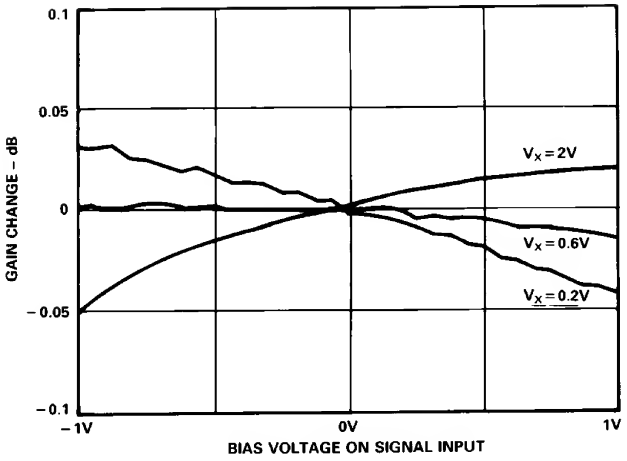

Figure 4. Differential Gain of the Voltage-Controlled Amplifier

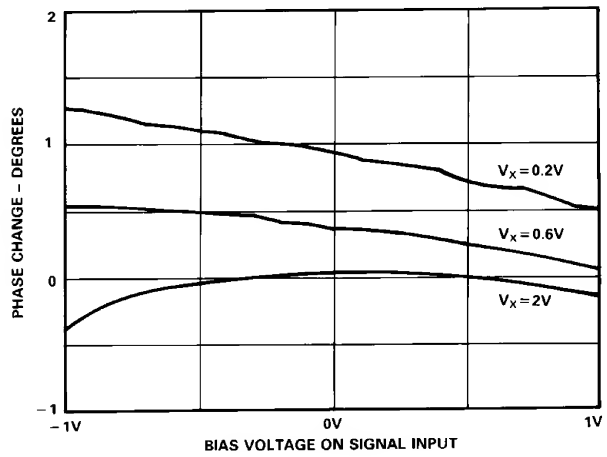

Figure 5. Differential Phase of the Voltage-Controlled Amplifier

In video applications, it is important that the gain and phase of the signal channels remain constant over the full-signal window. These aspects of the response are known as the differential-gain and differential-phase characteristics respectively, and are measured by superimposing a small AC signal at the subcarrier frequency (about 3.58MHz for NTSC systems) on top of a bias signal that modulates the channel over its nominal range, usually 0 to +1V. Figure 4 shows the variation in gain for $V_Y = -1V$ to +1V at a frequency of 3.58MHz, for three values of V_X. Figure 5 shows the phase variation under the same conditions. In most respects, this performance is similar to that which may be achieved using more expensive custom circuitry, although the control channel of the AD539 can be more easily overloaded by a rapidly-changing-step input.

A few final circuit details: in general, the control amplifier compensation capacitor for pin 2, C_C, must have a minimum value of 3000pF (3nF) to provide both circuit stability and maximum control bandwidth. However, if the *maximum* control bandwidth is not needed, then it is advisable to use a larger value of C_C, with typical values between 0.01 and 0.1μF. Like many aspects of design, the value of C_C will be a tradeoff: higher values of C_C will lower the high frequency distortion, reduce the high frequency crosstalk, and improve the signal channel phase response. Conversely, lower values of C_C will provide a higher control channel bandwidth at the expense of degraded linearity in the output response when amplitude modulating a carrier signal. The Control channel bandwidth will vary in inverse proportion to the value of C_C, providing a typical bandwidth of 2MHz with a C_C of 0.01μF and a V_X voltage of +1.7 volts.

Both the bandwidth and pulse response of the control channel can be further increased by using a feedforward capacitor, C_{ff}, with a value between 5 and 20 percent of C_C. C_{ff} should be carefully adjusted to give the best pulse response for a particular step input applied to the control channel. Note that since C_{ff} is connected between a linear control input (pin 1) and a logarithmic node, the settling time of the control channel with a pulse input will vary with different control input step levels.

Diode D1 clamps the logarithmic control node at pin 2 of the AD539, (preventing this point from going too negative); this diode helps decrease the circuit recovery time when the control input goes below ground potential.

THE AD539/5539 COMBINATION AS A FAST, LOW FEEDTHROUGH, VIDEO SWITCH

Figure 6 shows how the AD539/5539 combination can be used to create a fast video speed switch suitable for many high frequency applications including color key switching. It features both inverting and non-inverting inputs and can provide an output of ±1V into a reverse-terminated 75Ω load (or ±2V into 150Ω). An optional output offset adjustment is provided. The input range of the video switch is the same as the output range: ±1V at either input generates ±1V (noninverting) or ∓1V (inverting) across the 75Ω load. The circuit provides a dimensionless gain of about 1, when "ON", or zero when "OFF".

The differential configuration uses both channels of the AD539 not only to provide alternative input phases, but also to eliminate the switching pedestal due to step-changes in the output current as the AD539 is gated on or off.

The waveforms shown in Figures 7 and 8 were taken across a 75Ω termination; in both photos, the signal of 0 to +1V (in this case, an offset sine wave at 1MHz) was applied to the non-inverting input. In Figure 7, the envelope response shows the output being fully switched in about 50ns. Note that the output is ON when the control input is zero (or more negative) and OFF for a control input of +1V or more. There is very little control-signal breakthrough.

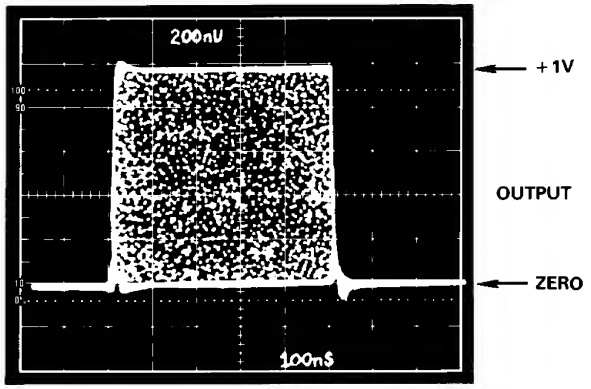

Figure 7. The Control Response of the Video Switcher

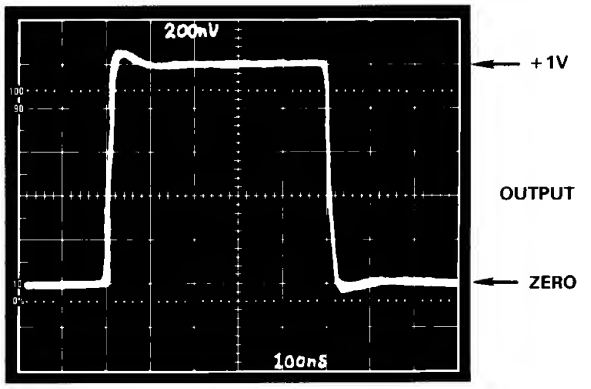

Figure 8. The Signal Response of the Video Switcher

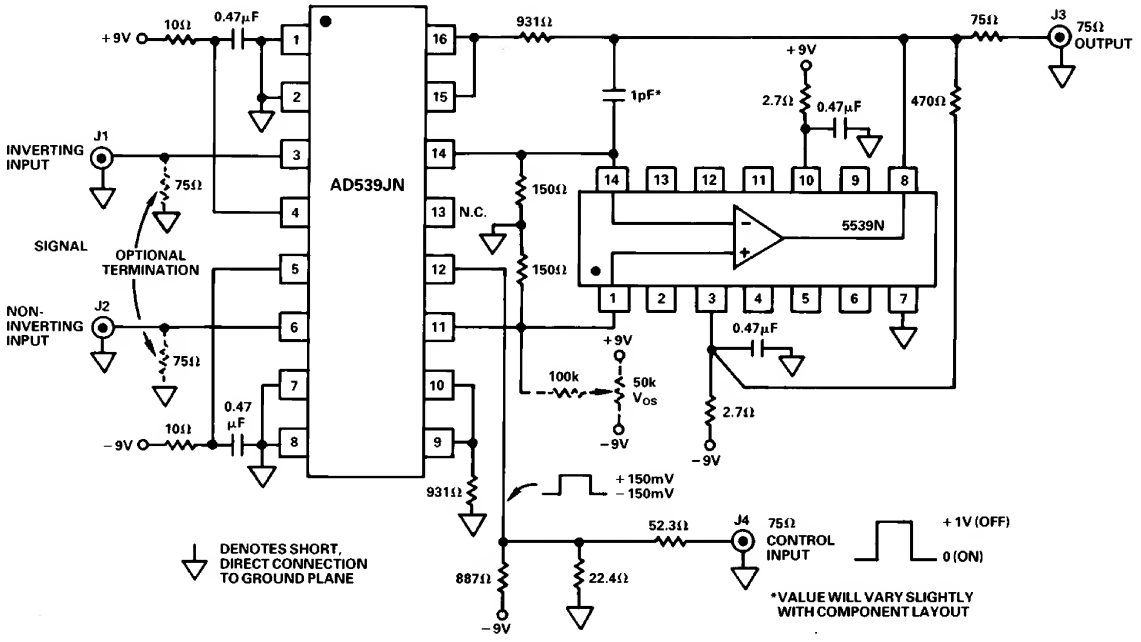

Figure 6. An Analog Multiplier Video Switch

Figure 8 shows the response to a pulse of 0 to +1V on the signal channel. With the control input held at zero, the rise-time is under 10ns. The response from the inverting input is similar.

The differential-gain and differential-phase characteristics of this switch are compatible with video applications. The incremental gain changes less than 0.05dB over a signal window of 0 to +1V, with a phase variation of less than 0.5 degree at the subcarrier frequency of 3.58MHz. The noise level of this circuit measured at the 75Ω load is typically 200μV in a 0 to 5MHz bandwidth or approximately 100nV per root hertz. The noise spectral density is essentially flat to 40MHz.

INSIDE THE AD539

Figure 9 is a simplified schematic outlining the main design features of the AD539 multiplier. Q1 through Q6, which form the translinear core of the multiplier, are multi-emitter NPN transistors having a very low base resistance, to minimize noise and distortion; emitter area scaling is also used in optimizing this crucial section of the circuit. Each of the pairs Q1-Q2, Q3-Q4, and Q5-Q6 form what is called a "controlled cascode" circuit; this is basically a grounded-base transistor to which has been added another device which removes some of the signal from the emitter. This alters the gain of the cascode, from almost unity (when *no* current is removed) to zero (when *all* the signal is removed). The "controlled cascode" configuration has very desirable characteristics for use in two-quadrant multiplication.

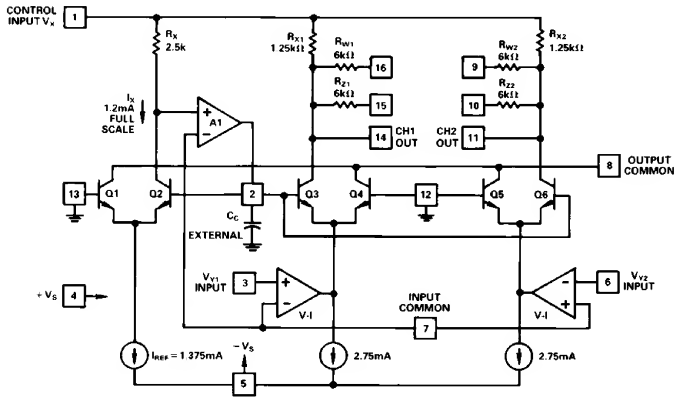

Figure 9. A Simplified Schematic of the AD539 Analog Multiplier

A stable 1.375mA reference current (which determines the multiplier scaling) is supplied to the common emitters of the controlled-cascode Q1-Q2, whose bases are biased by the control amplifier (a high-speed op-amp). When the control input V_X is zero, Q2 is biased off. This bias voltage is conveyed to Q3 and Q6, which are likewise turned off; signal transmission to the outputs is thus blocked. As V_X increases, the current through R_X (I_X) is forced to flow in the collector of Q2; this current only represents a fractional part of the 1.375mA reference current. When $V_X = 3V$ (its nominal full-scale value), 1.2mA flows in R_X and Q2; this is 0.873 (or 87.3%) of the reference current. Correspondingly, the *same fraction* of the signal and bias-currents that is supplied to the common emitter nodes of controlled cascodes Q3-Q4 and Q5-Q6 is conveyed to the two outputs.

Now consider the signals paths. The voltages V_{Y1} and V_{Y2} are converted to currents by V-I converters which have a transresistance of 1.74kΩ. At full-scale input of ±2V, the signal current supplied to the cascodes is ±1.15mA; this is superimposed on a bias current of 2.75mA. Thus, when $V_X = +3V$, the collector currents of either Q3 or Q6 will consist of a signal component of ±1mA (0.873 × 1.15mA) and a DC component of 2.4mA, both of these currents being proportionally less for other values of V_X. The DC component is removed by resistors R_{X1} and R_{X2}, driven directly from V_X. The final output is thus a current of value:

$$I_W = \frac{V_X}{1V} \times \frac{V_Y}{6k\Omega}$$

Note that the peak value of V_Y can be ±4.2V (using a $-V_S$ supply of at least −7.5V) and V_X can overrange by 10% to +3.3V, so the *peak* output current of each channel can be slightly more than ±2mA, for a maximum of ±4mA when the channels are used in parallel. These currents may be delivered directly to grounded load resistors or to terminated coaxial cables. With coaxial cables, the full 60MHz bandwidth of the AD539 can be realized, but the peak signal amplitude will be quite limited (to only ±330mV using a 75Ω load). Clearly, some additional gain is needed.

Unfortunately, the amplifiers necessary for additional gain could not be included on the AD539, due mainly to power dissipation considerations. Also, gain errors (of up to ±1.5dB) will occur using a simple load resistor, because of the 20 percent tolerance of the thin-film resistors. Fortunately, by using external op-amps, the output currents may be converted to much larger voltages, using on-chip applications resistors R_W and R_Z provided for this purpose. These resistors have a nominal value of 6kΩ, but they are laser-trimmed during manufacture so as to result in high gain-accuracy when used as the feedback resistors around an inverting op-amp. When using just R_W (R_{W1} for CH1, R_{W2} for CH2), the transfer characteristic becomes:

$$V_W = I_W \times R_W = \frac{V_X}{1V} \times \frac{V_Y}{6k\Omega} \times 6k\Omega = \frac{V_X V_Y}{1V} \text{ for } V_X > 0$$

When R_W and R_Z are used in parallel, the gain is halved, that is:

$$V_W = \frac{V_X V_Y}{2V}$$

The bandwidth is now largely determined by the op-amp. For wideband applications, the 5539N is an ideal low-cost complement to the AD539; this combination is capable of providing ±1V into a 75Ω load with only a very small degradation of the 60MHz bandwidth achieved by the AD539 alone.

LAYOUT OF VIDEO-BANDWIDTH CIRCUITRY

Careful component layout, adequate power supply bypassing, and proper coaxial cable termination are all very important in the implementation of video-bandwidth circuits in general. Unfortunately, even when these precautions are taken, some added difficulties can still arise in the case of voltage-controlled amplifiers. This can happen when leakage of the input signal to the output occurs when the gain should be zero. This feedthrough will cause ghost images which are generated by the high-frequency components of the unwanted signal.

A good ground plane is essential! To help assure this, it is recommended that part of this ground be run between the rows of the pins of both chips, on both the upper and lower surfaces of the PC board. The ground plane for a typical AD539/5539 layout is shown in Figure 10. In addition, all decoupling capacitors must have *minimum* lead lengths to this ground plane. Also, the input and output connections *must* be kept short, and should be physically separated as far as possible from each other. Separate power supply decoupling for the AD539JN and 5539N is also recommended.

Proper cable termination is also essential for adequate high-frequency performance. One-quarter-watt carbon resistors are well-suited for this function since they are non-inductive and quite inexpensive; one percent metal film resistors may also be used although their inductance should be measured first (since this property of the resistor may vary with each manufacturer). Avoid using wire wound resistors for termination!

The VCA described in this application note was designed to operate directly into a 75Ω load, therefore, "back-termination" (i.e., a series resistor which halves the load voltage) was not used. In most cases, the weak reflection from a short (up to 6 feet) directly-driven cable will not cause any visible effects. However, when using very long cables, it may be necessary to insert a 75Ω resistor in series with the output of the 5539N to absorb these reflections.

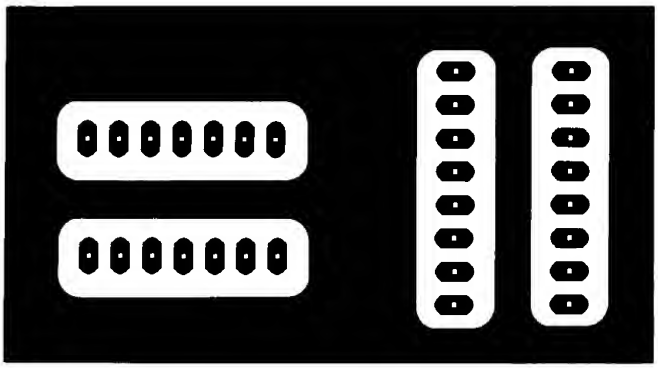

Figure 10. Layout of a Typical AD539/5539 Ground Plane

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